REMARKS

Applicants appreciate the examiner's allowance of Claims of 39-43, and traverse the rejections of the remaining Claims 1-38 and 44-63. Independent Claims 1, 16, 24, 31, 54 and 62 have been amended to improve their clarity and to better define the invention. For the reasons which follow, it is respectfully submitted that Claims 1-38 and 44-63 are patentable over the prior art of record. Accordingly, favorable reconsideration of this application and early allowance of all claims is respectfully requested.

I. The Rejection of Claims 1-2, 4, 6, 8, and 15 Under 35 U.S.C. §102(e)

The rejection of Claims 1-2, 4, 6, 8, and 15 as anticipated by U.S. Patent No. 6,785,290 to Fujisawa et al. is traversed. Independent Claim 1 has been amended to clarify that the method is performed by a storage switch and that packets are classified as data packets or non-data packets, and to further require that the recited steps be performed without buffering. For the reasons which follow, it is respectfully submitted that Fujisawa cannot anticipate Claim 1 or the claims dependent therefrom.

Fujisawa discloses an ATM switch for routing and switching ATM cells, i.e., packets, in an ATM communications network, that comprises line interface integrated circuits and a packet switch. ATM cells, i.e., packets, are supplied to an ingress line interface, temporarily stored in queues in a cell buffer according to classes which differ in priority, and are switched by a switch interface to an egress

line interface where they are further buffered until they are read out and routed to their designated destinations. Fujisawa discloses an ATM packet switch for a data communication network, not a storage switch in a storage network, as claimed. Moreover, ATM cells entering the line interfaces are buffered in cell buffers 24 (Figures 1, 3, 8B, 8C) 56, 66 (Figures 4, 8D) and 134 (Figure 10). Fujisawa explicitly discloses that all cells input to and output from the line interface circuits are buffered. (See, e.g., Column 3, lines 62-64; Column 4, lines 2-4 and 31-42; Column 7, lines 4-5; Column 9, lines 8-12; and Column 11, lines 52-53.)

Claim 1 requires that the steps of the claimed method be performed "without buffering". Since Fujisawa explicitly discloses cell buffers on the ingress and egress line interface circuits, and that these circuits buffer ingress and egress cells, Fujisawa cannot anticipate Claim 1, or any of the claims that depend therefrom. Accordingly, the rejection of Claims 1-2, 4, 6, 8, and 15 under 35 U.S.C. §102(e) as being anticipated by Fujisawa is improper and should be withdrawn.

Furthermore, for the reasons which will be discussed in more detail hereinafter, contrary to the Office's rejections, none of the other cited prior art of record, including U.S. Patent No. 6,621,818 to Szczepanek, discloses or suggests either methods for use by a storage switch, storage switches, or components thereof in which packets are processed without buffering. Accordingly, none of the other cited prior art either individually or in combination can render Claim 1 or any of the claims dependent thereon obvious and unpatentable under 35 U.S.C. §103.

Additionally, independent Claims 16, 24, 44, 50, 54, and 62 as well all require processing of packets "without buffering", and these independent claims and their corresponding dependent Claims 17-23, 25-30, 45-49, 51-53, 55-61, and 63 are likewise allowable over the prior art of record.

I. The Rejections Under 35 U.S.C. §103

Claim 3:

The rejection of Claim 3 under 35 U.S.C. §103(a) as unpatentable over Fujisawa in view of U.S. Patent No. 6,993,027 to Kadambi is traversed. Kadambi relates to a method of ordering frames in a local area data communications networks, i.e., LANs. Kadambi is concerned only with data communications network switches, not with storage switches for storage networks, as claimed, and does not address a storage switch or a storage network. Kadambi teaches a scheduler 99 that evaluates packets in queues in a FIFO 98 (i.e., a buffer), and schedules packets for transfer according to a scheduling algorithm (see Column 65, lines 40-60).

As is well known, there are significant differences between data communication networks and storage networks. Although data communications networks and storage networks both transfer data packets between devices, the issues faced by and processes employed in storage networks are substantially different from those faced by or employed in data communications networks. A storage network has much higher data integrity requirements and cannot afford to

lose data packets as can a data network in which lost packets can be retransmitted. Accordingly, references such as relating to data communication switches and networks have only limited relevance to storage networks. Moreover, Kadambi discloses buffering of packets. Accordingly, for the reasons discussed above with the respect to Claim 1, Fujisawa and Kadambi cannot in combination render either independent Claim 1 or dependent Claim 3 obvious.

III. Claims 5, 7, 9-12 and 14

The rejections of Claims 5, 7, 9-12 and 14 under 35 U.S.C.§103(a) as unpatentable over Fujisawa is traversed. These claims depend directly or indirectly from independent Claim 1, and are allowable over Fujisawa for at least the same reasons discussed above with respect to Claim 1.

Claim 5:

In addition, Claim 5 calls for a first and second device to both be included in the switch. In its rejection, the Office asserts that it would be obvious to implement devices internal or external of a switch, depending upon chip design requirements, and that it would be obvious to put the devices internal or external of the switch in a storage area network because it "could be possible" (emphasis added) to perform the recited task in a local network system.

It is respectfully submitted that this rejection is legally flawed and improper. The fact that it is "possible" to modify a reference to meet a claim is not sufficient to meet the Office's requirement to establish *prima facie* obviousness, and cannot be

used as a basis for supporting a rejection of that claim as being obvious over the reference. There must be a suggestion or motivation in the reference to make the modification. (See *in re Fritch*, 972 F 2d 1260 (Fed. Cir. 1992), MPEP §2143.01). There is nothing in Fujisawa that discloses or suggests the modification proposed by the Office in support of the rejection, and no motivation to make such a modification. Accordingly, the rejection of Claim 5 is improper.

Claim 7:

As to Claim 7, the rejection of this claim is also improper, for at least two reasons. First, the Office's assertion that a scheduler in a switch "could be used as a fabric" is baseless. There is nothing in the reference to suggest this, and it is contrary both to ordinary and customary meaning of the term "fabric" to one skilled in the art as well as to the teachings of the reference. Fujisawa teaches that the scheduler is used to read out cells that are stored in one of five queues in the cell buffers in accordance with their priority. A switch fabric, as is well known in the art, comprises a switch matrix which actually does the switching. There is no relationship between the scheduler of Fujisawa which schedules the order in which cells are read out of a buffer and a fabric, and the Office's assertion that Fujisawa's disclosure of a scheduler would make it obvious to use a fabric is unsupportable. Accordingly, the rejection of Claim 7 is improper.

Claims 9-11:

As to Claims 9-11, these claims depend directly or indirectly from Claim 1, and are deemed allowable for at least the same reasons discussed above that Claim 1 is allowable.

Claim 12:

As to Claim 12, as recognized by the Office Fujisawa does not teach virtualization. The Office's assertion that it would have been obvious to employ virtualization because virtualization is "often used" in packet switching systems and acts as "an awareness function" is both an incorrect interpretation of the claim language as well as a legally improper rejection. The term "virtualization" is defined by Applicants in the specification as referring to converting a virtual address to a physical address (see page 6, [0016] and page 14, [0063]). It is well established that claims must be read in the light of the specification, and that claim terms defined in the specification must be must given the meanings in the specification. Thus, the term virtualization in Claim 12 must be interpreted as that term as defined in the specification, which has nothing to do with an awareness function as asserted by the Office. Thus, the Office's interpretation of the claim and its rejection based upon this interpretation are improper. Furthermore, the rejection is legally flawed because the fact that something is "often used in a packet switching system" is not a sufficient basis for rejecting a claim in the absence of an explicit teaching or suggestion in the reference that the reference may be modified to include the

asserted function. There is no such teaching or suggestion in Fujisawa. Accordingly, the rejection of Claim 12 is improper.

Claim 14:

As to the rejection of Claim 14, Fujisawa does not disclose or suggest processing steps performed at "wire speed" as claimed. Because ATM systems transfer packets at the speed of the network is irrelevant. Claim 14 does not call for the transfer of packets in a network at wire speed. Rather, the claim calls for the processing of packets to be performed at "wire speed". The term "wire speed" is also explicitly defined in the specification at page 13, [0061] to mean that the storage switch introduces no more latency to a data packet during processed by the switch than would be introduced by a typical network switch performing switching functions, and gives examples of wire speed processing for different types of systems. There is no disclosure or suggestion in Fujisawa of processing packets at wire speed. In fact, processing at wire speed implies that there can be no buffering of packets, and Fujisawa explicitly discloses buffering of packets. Accordingly, the rejection of Claim 14 is improper.

IV. Claims 13, 16-23

The rejection of Claims 13 and 16-23 under 35 U.S.C. §103(a) as unpatentable over Fujisawa in view of U.S. Patent No. 6,621,818 to Szczepanek is traversed.

Claim 13 depends from Claim 1 and is deemed to be allowable for at least the same reasons discussed above that Claim 1 is allowable. Moreover, both independent Claims 1 and 16 call for the processing steps recited in those claims to be performed "without buffering". Szczepanek does not disclose or suggest processing of packets without buffering, as asserted, and even if combined with Fujisawa cannot render the claims obvious.

The Office's assertion that Szczepanek's teaching that buffering can be controlled depending upon bandwidth renders obvious the claims misconstrues the references and the claims. First, Szczepenak is concerned with a network switch in a data communications network that merely routes data packets, and Szczepenak explicitly teaches buffering of packets (See Column 6, lines 20-28; Column 7, lines 1-10; Column 8, lines 46-52 and Column 10, lines 5-15). The disclosure in Szczepanek at Column 10 that packet routing in a network switch may be without buffering if sufficient port bandwidth is available cannot render obvious the claimed method in a storage switch of a storage network in which the processing of packet includes receiving packets, classifying packets, and communicating packets, all without buffering, as set forth in independent Claims 1 and 16. Moreover, it is unclear as to how one would even combine Szczepenak with Fujisawa. Fujisawa deals with an ATM switch in which buffering is necessary in order to temporarily store ATM packets in different queues according to their priority so that they can be read out in priority sequence. Szczepenak merely relates to routing of packets without regard to priority, an approach that would not

be workable in the system disclosed by Fujisawa since packets could not be ordered according to priority without buffering.

Accordingly, it is submitted that Fujisawa and Szczepenak cannot be combined as asserted, and cannot render obvious Claims 13 and 16-23.

V. Claims 24-30, 44-49 and 50-61

The rejection of Claims 24-30, 44-49 and 50-61 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,647,019 to McKeown in view of Fujisawa and Szczepenak is traversed.

Independent Claims 24, 44, 50, and 54 are directed to either a method, a linecard or a switch, and all recite that data packets are processed "without buffering". As recognized by the Office, McKeown does not teach either classifying a packet into data or non-data packets, or processing packets without buffering. Fujisawa as explained above explicitly teaches buffering, and Szczepenak's teaching that buffering can be controlled in a router switch of a data network depending upon bandwidth does not disclose or suggest the processing of packets without buffering, as set forth in Independent Claims 24, 44, 50, and 54. As pointed out above in connection with the rejections of Claims 1 and 16, Szcepenak and Fujisawa cannot be combined because their teachings are incompatible, and even if they were combined, the combination would not produce the claimed invention since there would be no classification of packets or otherwise no processing of packets without buffering. Accordingly, it is respectfully submitted

that the rejection of Claims 24, 44, 50, and 54 as obvious over McKeown, Szcepenak and Fujisawa is improper, and that these independent claims are patentable over the cited prior art.

Dependent Claims 25-30, 45-49, 51-53 and 55-61 dependent from independent Claims 24, 44, 50 and 54, respectively, and are deemed to be allowable over the cited prior art for at least the same reasons that their corresponding independent claims are allowable. Moreover, these dependent claims set forth more specific features of the invention which also are neither disclosed nor suggested by the prior art.

Claim 26, for example, calls for the second device to which data packets are communicated to be on a linecard of a storage switch. Claim 28 calls for processing data packets in accordance with a virtualization function prior to communicating the data packets to the second device. Claim 29 calls for an identifier unit on the linecard to be a storage processor unit; and Claim 30 calls for the processing steps set forth in Claim 24 to be performed at wire speed.

All of these dependent claims are allowable over the prior art for at least the same reasons already discussed above. Furthermore, none of the prior art discloses or suggests a "second device" on a linecard of a storage switch, as claimed. Accordingly, the claims are allowable for this reason also.

Claims 45-46 are similar to Claims 25-27 and are deemed to be allowable for at least the same reasons. Claim 47 calls for data packets to include packets that are for an established connection and for a recognized protocol and are data

moving packets. Claim 48 calls for the linecard classifier to insert an indicator into a local header as to whether a packet is a data or non-data packet. The prior art of record neither discloses nor suggests the recitations of these claims.

Dependent Claims 51-53 are somewhat similar to dependent Claims 45-49 and are likewise deemed to be allowable for at least the same reasons. As to Claims 55-61, these claims are likewise similar to dependent Claims 25-30, 45-49, and 51-53, and are deemed to be allowable for at least the same reasons.

In view of the foregoing, it is submitted that the rejection of Claims 24-30, 44-49, and 50-61 is improper, and that these claims are allowable over the cited prior art.

VI. Claims 31, 33-38, and 62-63

The rejection of Claims 31, 33-38 and 62-63 under 35 U.S.C. §103(a) as unpatentable over McKeown, in view of U.S. Patent No. 6,292,489 to Fukushima and further in view of Fujisawa is traversed.

With respect to Claims 31 and 62, McKeown does not disclose a linecard in a storage network, but rather a linecard in a packet switch that includes buffering. Moreover, contrary to the Office's assertion, McKeown does not disclose identifying a data packet on a linecard. Rather, McKeown only identifies to a linecard whether a packet contains valid data in a particular field (see Column 6, lines 64-66). Identifying that a packet has valid data in a field has nothing to do with the claimed classification function of the invention.

Furthermore, Claim 31 has been amended to recite that all the processing steps set forth are performed without buffering, as previously recited in Claim 32. Similarly, Claim 62 has been amended to set forth that the software instructions on a medium in a storage switch operate without buffering of packets. For the reasons previous discussed above, the prior art of record does not disclose or suggest processing of data packets in a storage network without buffering of the packets. Accordingly, Claims 31 and 62, and the claims dependent thereon, are deemed allowable over the cited prior art. Dependent Claims 33-38 and 63 depend from Claims 31 and 62 and are deemed to be allowable for at least the same reasons that their corresponding independent claims are allowable.

VI. Claim 32

The rejection of Claim 32 as unpatentable over McKeown, Fukushima, Fujisawa, and Szcepanek is traversed.

Claim 32 depends from Claim 31 and is deemed allowable for the same reasons Claim 31 is allowable. Additionally, Claim 32 recites that the processing of packets, including classifying the packet, is performed in the linecard. None of McKeown, Fukushima, Fujisawa, and Szcepanek disclose or suggest classifying packets, much less classifying packets on a linecard. Accordingly, it is submitted that the cited prior art cannot render Claim 32 unpatentable, and that the claim is allowable.

In view of the foregoing, this application is now deemed to be in condition for allowance, and early allowance of all claims is respectfully requested.

The specification has been amended to update the status of the applications referenced on page 1.

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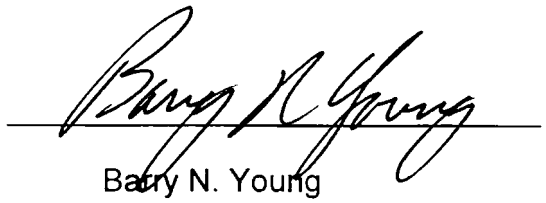
Respectfully Submitted,



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